IN THE CLAIMS

19. (Previously Presented) A memory device, comprising memory storage and three different interfaces to operate the memory storage in at least one of three different modes, wherein the memory storage and the three different interfaces reside in a common die.

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20. (Previously Presented) The memory device of claim 21, further comprising selection circuitry to select among the plurality of different interfaces.

21. (Previously Presented) The memory device of claim 19, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

22. (Original) The memory device of claim 21, wherein the memory device is a flash memory and the test interface is a standard flash memory interface.

23. (Original) The memory device of claim 21, wherein the operation interface is a proprietary interface.

24. (Previously Presented) The memory device of claim 20, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

25. (Canceled)

26. (Previously Presented) A component board, comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising memory storage and three different interfaces to operate the memory storage in at least one of three different modes, where in the memory storage and the three different interfaces reside in a common die.

27. (Previously Presented) The component board of claim 26, further comprising selection circuitry to select among the three different interfaces.

28. (Previously Presented) The component board of claim 27, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

29. (Previously Presented) The component board of claim 26, wherein the three different interfaces comprise:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

30. (Original) The component board of claim 29, wherein the memory device is a flash memory, the test interface is a standard flash memory interface, and the operation interface is a proprietary interface.

31. (Original) The component board of claim 27, wherein the memory device is a BIOS memory.

32. (Previously Presented) A computer system, comprising:

a peripheral device; and

a system board coupled to the peripheral device, the system board comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising memory storage and three different interfaces to operate the memory storage in at least one of three different modes, where in the memory storage and the three different interfaces reside in a common die.

33. (Previously Presented) The computer system of claim 32, further comprising selection circuitry to select among the three different interfaces.

34. (Previously Presented) The computer system of claim 33, wherein the selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

35. (Previously Presented) The computer system of claim 32, wherein the three different interfaces comprise:

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a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

36. (Original) The computer system of claim 35, wherein the memory device is a flash memory and the test interface is a standard flash memory interface and the operation interface is a proprietary interface.

37. (Original) The computer system of claim 33, wherein the memory device is a BIOS memory.

38. (Original) A memory device, comprising a plurality of different interfaces to operate the memory device in a plurality of different modes, wherein the memory device

is a flash memory and wherein one of the plurality of interfaces is a standard flash memory interface.

Claims 39-41 (Canceled)